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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,021	FELDMAN, ARNOLD R.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,16,18-22,26 and 28-30* is/are rejected.

7)☒ Claim(s) *3, 6, 17, 23-25, and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawings

The amendment and drawings corrections submitted on May 17, 2002 have been reviewed and considered with the following results:

The proposed drawing changes, along with associated changes within the specification, have overcome the objections described in the previous Office Action. Therefore, those objections have been withdrawn.

Similarly, the amended changes to the specification overcame the disclosure's objections, which have also been withdrawn.

The cancellation of claims 7-15 rendered all of their respective objections and rejections moot. However, newly added claims 24 and 25 have their own objections that are described later under the appropriate section.

Amended claim 1 overcomes the rejections of claims 1-6 under 35 U.S.C. 112. The claim no longer recites an "RF signal" on line 1 and "an input signal" on line 2. Therefore, those rejections have been withdrawn.

After considering the applicants arguments/comments with respect to the Hoover reference, the rejections of claims 1-6 under 35 U.S.C. 102(b) have been withdrawn. Hoover does not clearly show or disclose the first and second currents being approximately zero, as recited within claim 1 since Hoover identifies the operation of the circuit as a Class A amplifier. These prior art rejections have been withdrawn.

The rejections of claims 1-6 and 16 under 35 U.S.C. 102(b), and of claims 17-21 under 35 U.S.C. 103(a), with respect to the Gabara reference, have all been withdrawn.

As pointed out by the applicant, and inadvertently overlooked by the examiner, transistors 30p and 32p receive a common control voltage Vpch instead of complementary signals. Thus, voltage Vpch is not a signal that alternates between first and second polarities as recited within claim 1. Also, since the transistors share a common input, the reference does not clearly show or disclose the control electrodes of transistors 30p and 32p connected to their respective first and second input nodes as recited within claim 16.

Although all the original objections and rejections have been withdrawn as described above, various new objections/rejections are described below under their respective sections. Also, comments related to the applicant's arguments or comments are described under the Response to Arguments section.

Claim Objections

Claims 24 and 25 are objected to because of the following informalities: Claim 24, line 1 "the input signal" should be --the RF signal-- to clearly correspond to the signal recited within claim 22. Similarly, each of the four occurrences of "the RF signal" on lines 2-4 of claim 25 should be --the RF signal--. Appropriate corrections are required.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Luu, a reference found during a recent search. The circuit shown in Luu's Fig. 2 provides a method for buffering an RF signal. The method comprises: 1) receiving an RF signal (from RF source 20 shown in Fig. 1), at 100, that alternates between first and second polarities (e.g. see column 4, lines 25-43); 2) generating a first current, by transistor 70, that is proportional to the RF signal at a first polarity (that causes the transistor to conduct), wherein the first current is approximately zero when the RF signal has a second polarity (causing transistor 70 to turn off); 2) generating a second current, by transistor 774, that is proportional to the RF signal at its second polarity (that causes the transistor to conduct), wherein the second current is approximately zero when the RF signal has the first polarity (causing transistor 74 to turn off); 3) using the first current (from transistor 70) to generate a third current (through a conducting transistor 76) that is proportional to the first current; 4) using the second current (from transistor 74) to generate a fourth current (through a conducting transistor 72) that is proportional to the second current; 5) applying the first and fourth currents to a first terminal J1 of inductor

44; and 6) applying the second and third current to a second terminal J2 of inductor 44, anticipating claims 1 and 22. [Note that Luu discloses transistors 70,76 are on while transistors 72,74 are off (e.g. see column 4, lines 42-43). For example, one of ordinary skill in the art would know a current flows from B+ to ground through 70, 44, and 76 when transistors 70 and 76 are conducting, and no (or approximately zero) current would flow through transistors 74 and 72 because they would be off. Although the current flowing through each transistor (e.g. 70 and 76) is considered here as a separate current, one of ordinary skill in the art would know the first current (through transistor 70) would be the same as, or equal to, the fourth current (through transistor 76), and therefore they would be proportional.]

Claims 1, and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al. (Horiguchi), another reference found during a recent search. Fig. 6 of Horiguchi shows a circuit comprising a well-known H-bridge (or full-bridge) circuit that closely corresponds to the applicant's Fig. 3 RF buffer amplifier. For example, Horiguchi's transistors Q1,Q2,Q4,Q3, first supply node (i.e. the top of power supply 9), first output node (i.e. the common connection between Q1 and Q4), second output node (i.e. the common connection between Q2 and Q3), second supply node (i.e. ground), inductor L, and capacitor C respectively correspond to the applicant's switches S1-S4, first supply node 360, first output node 390, second output node 380, second supply node 370, inductor L1, and capacitor C1, respectively. Therefore, a more detailed description of the structure is not necessary to one of ordinary skill in the art with respect to the applicant's claimed circuit. In operation, first/ fourth switches Q1/Q3 of

Horiguchi's circuit are closed while the second/third switches Q2/Q4 are open, and vice versa. The opening and closing of the switches depend upon the polarity of input signal VT shown in Fig. 1. [Fig. 1 corresponds to block 2 in Fig. 6.] The input signal's polarity alternates between increasing and decreasing (see column 8, lines 25-32 and Fig. 2). For example, at a first polarity, transistors Q1 and Q3 will conduct, and current 6_1 will flow from 9 to ground through L,C in one direction, wherein at a second polarity, transistors Q2 and Q4 will conduct, and current 6_2 will flow from 9 to ground through L,C in the opposite direction. See column 6, lines 51-60. From the disclosure on column 6, lines 34-39, one of ordinary skill in the art would recognize Horiguchi's Q1,Q3 are conducting when Q2,Q4 are off, and vice versa. Therefore, a first current 6_1 (generated by Q3) will be proportional to the input signal when it is at the first polarity allowing Q3 to conduct, wherein first current 6_1 will be approximately zero when the second polarity turns Q3 off; a second current 6_2 (generated by Q4) will be proportional to the input signal that is at the second polarity allowing Q4 to conduct, wherein second current 6_2 will be at approximately zero when the first polarity turns Q4 off; Q1 generates a third current 6_1 proportional to first current 6_1; Q2 generates a fourth current 6_2 proportional to second current 6_2; the first current 6_1 (from Q3) and the fourth current 6_2 (from Q2) are applied to the first terminal (i.e. shown at the right side) of inductor L; and the second current 6_2 (from Q4) and the third current 6_1 (from Q1) are applied to the second terminal (i.e. shown at the left side) of inductor L. Thus, the limitations of claim 1 are anticipated. Since inductor L and capacitance C are coupled in parallel, they form a tank circuit, anticipating claim 2.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (Horiguchi) in view of claims 1 and 2 described previously. Although Horiguchi shows/discloses a method for generating first-fourth currents with respect to an inductor (as recited within claims 1 and 2), the reference does not show the first/second currents as being generated by NMOS devices, and the third/fourth currents as being generated by PMOS devices. However, those currents are shown generated by NPN and PNP devices, respectively and Horiguchi discloses (on column 14, lines 35-37) that the inductive load driving method and H-bridge circuit control device can use MOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art to replace the NPN (Q4,Q3) and PNP (Q1,Q2) transistors of Horiguchi's H-bridge circuit (in Fig. 6) with respective corresponding NMOS and PMOS transistors. Since the first/second currents would then be generated by NMOS devices, and the third/fourth currents would then be generated by PMOS devices, claims 4 and 5 would be rendered obvious. MOS devices can be used for easier fabrication of the circuitry, and they would help reduce power consumption of the entire circuit if that was desired.

Claims 1, 16, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maggio et al. (Maggio), a reference cited in the previous Office

Action. In Fig. 3, Maggio shows a circuit comprising a first device 304 coupled between a first output node HY and a first supply node, and having a control electrode (i.e. gate); a second device 302 coupled between a second output node HX and first supply node VDD, with a control electrode (i.e. gate; a third device Q1 coupled between a second supply node (e.g. ground) and first output node HY, with its control electrode (i.e. base) coupled to second output node HX; a fourth device Q2 coupled between the second supply node and second output node HX, with its control electrode coupled to first output node HY; and write head (not labeled) coupled between the first/second output nodes HY/HX. Although the reference does not clearly disclose the write head as an inductor, it discloses "the write head is an inductive load" (see column 4, line 1). Therefore, one of ordinary skill in the art can deem the write head, an inductive load, as one type of inductor. Also, although the reference does not clearly show first/second input nodes as being coupled to the control electrodes of the respective first/second devices 304/302, one of ordinary skill in the art would know they must be connected to some type of input/node, wherein Maggio does disclose the gates of 302 and 304 are connected to control circuitry (e.g. see column 4, lines 8-12). Since one of ordinary skill in the art would know both devices 302 and 304 would not be turned on at the same time, their respective gate must receive different (e.g. complementary signals). Therefore, the gate of device 304 can be deemed coupled to a first input node with respect to the control circuitry, while the gate of device 302 can be deemed coupled to a second input node with respect to the control circuitry, thus rendering claim 16 obvious. Maggio discloses all the transistors within the H-bridge circuit 300 (i.e. Fig. 3) could be

FETs (see column 3, lines 58-62). Therefore, it would be obvious to replace NPN transistors Q1 and Q2 with corresponding FETs (i.e. NMOS). Fig. 3 is one type of a differential amplifier. In this case, PMOS transistors 304/302 function as the amplifier's input transistors. However, NMOS transistors can also be used as input transistors. Although Fig. 3 shows the two PMOS input transistors 304,302 receiving the first/second input signals, and the two NMOS transistors 308,306 would be the cross-coupled transistors, it would be obvious to one of ordinary skill in the art to modify the configuration to have the NMOS transistors serve as the differential pair receiving the first/second input transistors, and the PMOS transistors would be cross-coupled. Therefore, the first/second devices would now be NMOS transistors 308/306, and the third/fourth devices 304/302 would be PMOS transistors, rendering claim 18 obvious. Since the circuit of Fig. 3 comprises mainly semiconductor devices, it would be obvious to one of ordinary skill in the art to form the elements on an integrated circuit (IC), rendering claim 19 obvious. Integrated circuits help to keep the size of overall circuits or systems small, with reduced energy consumption. Fig. 1 of Maggio can be considered one type of computing device. As disclosed on column 3, lines 10-12, controller unit 160 comprises a memory and central processing unit, and block 190 can be deemed a transceiver since it would be used to transmit (write) data, and receive (read) data. When it is used to write data, it relates to the circuit of Fig. 3, thus the transceiver can be considered as comprising the circuit of claim 18, rendering claim 20 obvious. As shown in Fig. 1, transceiver 190 is coupled to controller unit 160. Therefore, it would be obvious to one of ordinary skill in the art that transceiver 190

would be also coupled to the central processing unit, either directly or indirectly, rendering claim 21 obvious. The transceiver (read/write channel) 190 requires control, and this can be performed by the CPU. In operation, transistors 304 and 302 receive an input signal that allows them to operate in a complementary manner (e.g. see column 3, lines 56-58 and 62-64). When conducting, the current of a transistor can be considered proportional to its input signal. Therefore, assume a first polarity of the input signal turns transistor 304 on, which then generates a first current, wherein the first polarity turns transistor 302 off, which would then generate approximately zero (or no) current. The second polarity of the input signal would turn transistor 302 on, which then generates a second current, wherein the second polarity would turn transistor 304 off, which would then generate approximately zero (or no) current. With transistor 304 on, transistor Q2 (306) would turn on and generate a third current proportional to the first current since the current(s) flows from VDD through 304, the inductor, and Q2 (306) to ground. Also, when transistor 302 turns on, transistor Q1 (308) would turn on and generate a fourth current proportional to the second current since these currents would relate to the current flowing from VDD to ground through 302, the inductor, and Q1 (308). The first and fourth currents (related to 304 and Q1 (308), respectively) are applied to a first terminal HY of the inductor, and the second and third currents (related to 302 and Q2 (306), respectively) are applied to a second terminal HX of the inductor. Therefore, claim 1 is anticipated.

Independent claims 22, and 26 (along with dependent claims 28-30) are rejected under 35 U.S.C. 103(a) as being unpatentable over Maggio et al. (Maggio) as applied to

respective independent claims 1 and 16 (along with dependent claims 18-20) above, and further in view of Maletsky et al. (Maletsky). Method claims 1 and 22 are almost identical with one major exception, claim 1 only recites an "input signal", wherein claim 22 now identifies the signal as an "RF signal." [Also, two minor changes within the claims were also noted: Claim 1 generates a third (fourth) current proportional to the first (second) current, while claim 22 uses the first (second) current to generate the proportional third (fourth) current. Since one of ordinary skill in the art would know that if there is no first (second) current, there could be no third (fourth) current. Therefore, the generation of the proportional currents in claim 1 is considered directly related to the use of the first/second currents to generate their respective third/fourth current as recited within claim 22.] Maggio does not clearly show or disclose the input signal for controlling transistors 304 and 302 as RF signals. However, Maggio does relate Fig. 3 with a write head (the inductor as previously described) and a controller 160 having a CPU, memory, etc. Therefore, it is clear the circuit of Maggio relates to a memory device for writing data. Maletsky discloses writing requests are communicated by radio frequency signaling (e.g. see the reference's claim 15). Therefore, it would have been obvious to one of ordinary skill in the art to use RF signals as the input signals for Maggio's circuit, thus rendering claim 22 obvious. At RF signal frequencies, the circuit of Maggio would operate at those frequencies, if that frequency (speed) was desired. With respect to claims 16 and 22, claim 22 now identifies an RF signal is received at the control electrode of the first device, and a complement of the RF signal is received at the control electrode of the second device, wherein claim 16 only indicated the control

electrodes were coupled to their respect first and second input node. Therefore, assuming the control electrodes (i.e. gates) of Maggio's transistors 304 and 302 receive RF signals as described above, one of ordinary skill in the art would know they would have to be complementary (e.g. high and low) in order to provide the proper operation of the circuit (e.g. 304,306 are on while 302,308 are off, and vice versa). Therefore, if the RF signal causes 304 to generate a first conduct current, the complementary RF signal would cause 302 to generate approximately zero current because transistor 302 would be turned off. Similarly, if the absence of the RF signal causes 304 to turn off and generate approximately zero current, the complementary RF signal would cause 302 to turn on and generate a second current. Therefore, independent claim 26, and its dependent claims 28-30, are also rendered obvious.

No claims are allowable as presently written.

However, claims 3, 6, 17, 23-25, and 27 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the circuit, amplifier and/or method comprise the: 1) first and second frequencies as recited within claim 3, or the geometrically proportional currents as recited within claim 6, where both claims depend on claim 2 that has a tank circuit formed by the inductor and capacitance; 2) fifth and sixth devices as recited within claims 17 and 27; 3) the method for generating first-fourth currents, related to an inductor, also includes a tank circuit formed by the inductor and a capacitance as recited within claim 23 (upon which

claim 24 depends); and 4) the currents are geometrically proportional as recited within claim 25.

Claims 7-15 have been canceled.

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. For example, although not used in any formal rejections described above, it is suggested all these references be carefully reviewed and considered with respect to the limitations recited within at least the independent claims. Fig. 1 of Yamaguchi shows a circuit in Fig. 1 with four devices that would each generate its own current. If an inductor would be added between outputs N21 and N22, and respective cascode transistors would be added between transistors 1,(2) and output N21 (N22), the circuit would correspond to the elements M2-M7,L1 shown in the applicant's own Fig. 4. Also, Yamaguchi shows a circuit in Fig. 8 that closely corresponds to the transistor structure of Maggio et al. (identified above under the rejections), with a pair of input transistors and a pair of cross-coupled transistors connected to the outputs. Fig. 8 of Yamaguchi shows another embodiment, wherein the input transistors and cross-coupled transistors have been reversed with respect to their connections and types. Other than lacking an inductor between the two output nodes, Figs. 1 and 2 of Briner closely correspond to the applicant's Fig. 4, including at least two cascode transistors (not labeled in Figs. 1 and 2), but corresponding to at least transistors 52, and 56 of Briner's Fig. 3. These cascode transistors function as guard devices, helping to prevent snapback. Krishnamurthy et al. shows examples of amplifier circuits having PMOS input transistors M2,M3 and cross-coupled NMOS transistors

M7,M8 in Fig. 2, wherein Fig. 3 shows NMOS input transistors M12,M13 and cross-coupled PMOS transistors M17,M18. Therefore, this reference provides motivation/teachings for using either configured circuit (i.e. PMOS input vs. NMOS input). Figs. 1 and 2 of Chen et al. clearly show a circuit comprising four devices MP1,MP2,MN1,MN2 for generating respective currents, which are applied to an inductor L1.

The prior art reference cited on the IDS submitted Jun 17, 2002 was reviewed and considered. It does not clearly show or disclose the claimed limitations related to either: 1) the first-fourth currents and the inductor as recited within independent method claims 1 and 26; or 2) the first-fourth devices and inductor as recited within independent apparatus claims 16 and 26.

The applicant's co-pending application, now identified on page 13 as 09/836,624, was retrieved and reviewed. None of its claims recite an inductor, nor do they recite the first-fourth currents and/or devices with respect to the inductor as each of the independent claims of the present application recites. Also, none of the figures correspond to Figs. 3 and 4 of the present application, which in turn correspond to the claimed limitations of the present application. Therefore, applications 09/835,021 and 09/836,624 two presently recite distinct inventions.

Response to Arguments

The applicant's arguments filed May 17, 2002 have been fully considered but they are not persuasive. The applicant argues: 1) the method of buffering an input signal saves power; and 2) the current, as claimed, is proportional to the input signal.

1) The applicant's argument with respect to "buffering an input signal" and "buffering RF signals" fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. If a circuit provides an output signal in response to an input signal, the circuit can be considered one type of a buffering circuit for that particular input signal. Also related to this, in response to the applicant's argument that a reference (i.e. Hoover) fails to show a certain feature of the applicant's invention, it is noted that the feature upon which the applicant relies (i.e., buffering an input signal to save power) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

2) The applicant's arguments do not comply with 37 CFR 1.111(c) because the rejected claims do not clearly point out the patentable novelty with respect to what the applicant thinks a proportional current is that the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. When a transistor begins to conduct current due to the transistor's input signal, that current can be considered proportional to the input signal (e.g. with a sufficient input signal, the transistor will allow current to flow). Also, when a transistor turns off, or nears turn off, due to the transistor's input signal, that current is approximately zero (assuming some leakage current or incomplete turn off). For example, when Horiguchi's current 6_1

passes through transistors Q1 and Q3 when they are conducting, the current through Q1 can be considered one current, and the current through Q3 can be considered another current. However, those currents are proportional to one another because they are equal (i.e. a 1:1 ratio), and they are proportional to the input signal that allows the transistors to conduct and current to flow. When transistors Q1 and Q3 are turned off, current 6_1 will not flow. Therefore, at that time current 6_1 will, or will approximately, be zero.

Therefore, the rejections are deemed proper.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

19 July 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800